Remarks

Applicants respectfully request reconsideration of the present application in view of the foregoing amendments and following remarks. Claims 1-30, 32, and 34-37 remain pending in the current application. Claims 4, 30, 32, 35, and 36 have been amended to address minor informalities and not for reasons related to patentability. For example, an extraneous "the" was removed from the preamble of claim 4 and, in claim 32, "acombined" was changed to correctly read "a combined." Also, the second claim 32 has been canceled and a corresponding claim is presented as new claim 37, depending from claim 30. Claims 35 and 36 have been amended to properly depend from claim 34 instead of claim 26. In addition, the first claim 32 has been amended to properly depend from claim 30 instead of claim 31. Claim 30 has been amended to incorporate the limitations of claims 31 and 33. Accordingly, claims 31 and 33 have been canceled.

I. Claim Rejections under 35 U.S.C. § 102

The Office Action stated that claims 1-3, 8, and 12 are rejected under 35 U.S.C. § 102(e) as being anticipated by the example prior art testing environment of FIG. 1 and description ("FIG. 1 Art").

These rejections are respectfully traversed.

Independent claim 1 is directed to a circuit for testing multiple memories, and requires: "a resume input on the integrated circuit for receiving a signal, the resume input coupled in parallel to the two or more BIST controllers, wherein the two or more BIST controllers are responsive to the signal on the resume input to exit an idle state" (emphasis added). For example, FIG. 3 of the

present application shows a single resume pin 108 that is coupled in parallel to the 1st 90 through Nth 92 BIST controllers.

The FIG. 1 Art fails to teach or suggest a circuit having a resume input on the integrated circuit for receiving a signal, the resume input coupled in parallel to the two or more BIST controllers, such as that recited in independent claim 1. The present application describes FIG. 1 at page 3, lines 6-23:

> FIG. 1 shows an example prior art testing environment 10 for testing embedded memories that includes automated test equipment (ATE) 12 coupled to an IC 14. The IC 14 includes N BIST controllers (shown generally at 16) coupled in parallel. Each BIST controller is coupled to multiple memories to be tested. For example, a BIST controller 18 is coupled to the memories through data, address, and control lines. The memories 18, 20, 22 are shown having one or more output buses (shown generically at 26) coupled to the BIST controller 18. In the case where each memory has a separate output bus, the BIST controller 18 tests memories 20, 22, 24 in parallel and is called a "parallel" BIST controller. In the case where each memory has a shared output bus or the power budget prevents testing in parallel, the BIST controller 18 tests the memories one at a time (i.e., sequentially) and is called a "sequential" BIST controller.
>
> To properly test the memories using retention or IDDQ tests, **each BIST controller is coupled to a separate "hold" pin, such as hold pins 30, 32, on the IC 14.** The hold pins are coupled to the ATE 12, which controls each hold pin individually. For example, when the ATE determines that BIST controller 18 is ready for a retention or IDDQ test, the hold pin 30 is asserted causing the BIST controller 18 to remain idle. The ATE then waits the desired amount of time and deactivates the hold pin allowing the BIST controller to continue the memory tests. (emphasis added)

While the FIG. 1 Art does show separate "hold" pins for each BIST controller, it explicitly lacks any type of resume pin for any of the N BIST controllers, much less a resume pin coupled to multiple BIST controllers. Therefore, the FIG. 1 Art fails to teach or suggest "a resume input on the integrated circuit for receiving a signal, the resume input coupled in parallel to the two or more BIST controllers, wherein the two or more BIST controllers are responsive to the signal on the resume input to exit an idle state," as recited in independent claim 1. Accordingly, Applicants respectfully request that the 35 U.S.C. § 102(e) rejection be withdrawn from independent claim 1.

Dependent claims 2, 3, 8, and 12 depend directly or indirectly from independent claim 1 and are allowable for at least the reasons recited above in support of their parent claim 1. They are also independently patentable. Accordingly, the 35 U.S.C. § 102(e) rejections of claims 2, 3, 8, and 12 should be withdrawn.

II. Claim Rejections under 35 U.S.C. § 103

The Office Action stated that claims 4-7, 9-11, and 13-36 are rejected under 35 U.S.C. § 103(a) as being unpatentable over the FIG. 1 Art in view of U.S. Patent No. 6,651,202 to Phan ("Phan").

The Office Action also stated that claims 4-7, 9-11, and 13-36 are rejected under 35 U.S.C. § 103(a) as being unpatentable over the FIG. 1 Art in view of U.S. Patent No. 6,415,403 to Huang et al. ("Huang").

These rejections are respectfully traversed.

a. Claims 4-7 and 9-11

Dependent claims 4-7 and 9-11 depend directly or indirectly from independent claim 1 and are allowable for at least the reasons recited above in support of their parent claim 1. They are also independently patentable. Accordingly, the 35 U.S.C. § 103(a) rejections of claims 4-7 and 9-11 should be withdrawn. Neither Phan nor Huang cure the deficiencies of the FIG. 1 Art.

b. Claims 13-18

Independent claim 13 is directed to a circuit for testing multiple memories, and requires: "at least one BIST controller within an integrated circuit, wherein the BIST controller has a

synchronization output which is activated when the controller is in an idle state" (emphasis added). For example, FIG. 3 of the present application shows synchronization outputs 101 and 103 from BIST controllers 90 and 92, respectively. The present application describes exemplary synchronization outputs at page 3, line 25, to page 4, line 3:

> The BIST controllers 88 have synchronization feedback outputs, such as 101 and 103 from BIST controllers 90, 92, respectively. The synchronization feedback outputs 101, 103 carry signals indicating that their respective controller is in a synchronization state. For example, synchronization output 101 is activated (i.e., may be active high or low) when the BIST controller 90 has completed a phase of the memory test.

The FIG. 1 Art fails to teach or suggest a circuit having at least one BIST controller within an integrated circuit, wherein the BIST controller has a synchronization output which is activated when the controller is in an idle state, such as recited in independent claim 13. For example, the FIG. 1 Art does not show or suggest any type of synchronization output from any of the N BIST controllers. Furthermore, the FIG. 1 Art does not show or suggest any type of output from any of the N BIST controllers while the controller is in an idle state. Therefore, the FIG. 1 Art fails to teach or suggest "at least one BIST controller within an integrated circuit, wherein the BIST controller has a synchronization output which is activated when the controller is in an idle state," as recited in independent claim 13.

Phan does not cure the deficiencies of the FIG. 1 Art. Phan also fails to teach or suggest a circuit having at least one BIST controller within an integrated circuit, wherein the BIST controller has a synchronization output which is activated when the controller is in an idle state, such as recited in independent claim 13. For example, "FIG. 1 [of Phan] provides a simplified schematic diagram of an exemplary integrated circuit IC incorporating testing and repair capabilities capable of being utilized in conjunction with the present invention...The integrated circuit IC comprises a built-in self-test (BIST) state machine/controller 102 for controlling the

various other components of the disclosed memory BIST system" (Phan at col. 5, lines 10-13 and 17-20, respectively). The Office Action noted the only reference understood to be present in Phan to anything related to synchronization: "A system clock signal SYSTEM_CLOCK is also **provided to** both **the BIST state machine controller 102** and the BISR circuitry 110 for logic clocking and synchronization" (Phan at col. 6, lines 57-60, emphasis added). The system clock signal is provided as an **input** to the BIST controller and, therefore, **cannot be an output** from the BIST controller. Furthermore, Phan is not understood to deal with anything related to idle states. A simple key word search for the word "idle" within Phan returned zero results. Therefore, Phan fails to teach or suggest "at least one BIST controller within an integrated circuit, wherein the BIST controller has a synchronization output which is activated when the controller is in an idle state," as recited in independent claim 13. Therefore, Phan cannot cure the deficiencies of the FIG. 1 Art. Accordingly, Applicants respectfully request that the 35 U.S.C. § 103(a) rejection based upon the FIG. 1 Art and Phan be withdrawn from independent claim 13.

Huang also does not cure the deficiencies of the FIG. 1 Art. Huang also fails to teach or suggest a circuit having at least one BIST controller within an integrated circuit, wherein the BIST controller has a synchronization output which is activated when the controller is in an idle state, such as recited in independent claim 13. The Office Action noted the only reference understood to be present in Huang that has anything related to synchronization: "All signals are synchronized **with the BIST clock**, BCK" (Huang at col. 5, line 65, emphasis added). FIG. 1 of Huang and related description describe the clock signal as an **input** to the BIST controller and, thus, not an **output** from it. Furthermore, Huang does describe a BIST moving between an idle state and a reset state but is understood to not disclose any output, much less any type of

synchronization output, that is activated when a BIST controller is in an idle state. Therefore, Huang fails to teach or suggest "at least one BIST controller within an integrated circuit, wherein the BIST controller has a synchronization output which is activated when the controller is in an idle state," as recited in independent claim 13. Therefore, Huang cannot cure the deficiencies of the FIG. 1 Art. Accordingly, Applicants respectfully request that the 35 U.S.C. § 103(a) rejection based upon the FIG. 1 Art and Huang be withdrawn from independent claim 13.

Because each of the cited references, individually and in combination, fails to teach or suggest "at least one BIST controller within an integrated circuit, wherein the BIST controller has a synchronization output which is activated when the controller is in an idle state," as recited in independent claim 13, the 35 U.S.C. § 103(a) rejections should be withdrawn.

Dependent claims 14-18 depend from independent claim 13 and are allowable for at least the reasons recited above in support of their parent claim 13. They are also independently patentable. Accordingly, the 35 U.S.C. § 103(a) rejections of claims 14-18 should be withdrawn.

c. Claims 19-29

Independent claim 19 is directed to a method of testing memory, and requires: "asserting a synchronization signal indicating that the group of memories are at a common synchronization state."

The FIG. 1 Art fails to teach or suggest a method of testing memory requiring asserting a synchronization signal indicating that the group of memories are at a common synchronization state, such as recited in independent claim 19. For example, the FIG. 1 Art does not show or suggest any type of synchronization signal. Furthermore, the FIG. 1 Art does not show or suggest any type of synchronization states of memories. Therefore, the FIG. 1 Art fails to teach

or suggest "asserting a synchronization signal indicating that the group of memories are at a common synchronization state," as recited in independent claim 19.

Phan does not cure the deficiencies of the FIG. 1 Art. Phan also fails to teach or suggest a method of testing a group of memories requiring asserting a synchronization signal indicating that the group of memories are at a common synchronization state, such as recited in independent claim 19. The only reference understood to be present in Phan to anything related to synchronization is as follows: "A **system clock signal** SYSTEM_CLOCK is also provided to both the BIST state machine controller 102 and the BISR circuitry 110 for logic clocking and synchronization" (Phan at col. 6, lines 57-60, emphasis added). Thus, Phan describes a system clock signal that is input to a BIST but is understood to disclose nothing relating to any type of common synchronization state between memories, much less asserting any type of signal indicating that memories are at a common synchronization state. Therefore, Phan fails to teach or suggest "asserting a synchronization signal indicating that the group of memories are at a common synchronization state," as recited in independent claim 19. Therefore, Phan cannot cure the deficiencies of the FIG. 1 Art. Accordingly, Applicants respectfully request that the 35 U.S.C. § 103(a) rejection based upon the FIG. 1 Art and Phan be withdrawn from independent claim 19.

Huang also does not cure the deficiencies of the FIG. 1 Art. Huang also fails to teach or suggest a method of testing a group of memories requiring asserting a synchronization signal indicating that the group of memories are at a common synchronization state, such as recited in independent claim 19. The only reference understood to be present in Huang to anything related to synchronization is as follows: "All signals are synchronized **with the BIST clock**, BCK" (Huang at col. 5, line 65, emphasis added). Thus, Huang describes a clock signal that is input to

a BIST but is understood to disclose nothing relating to any type of common synchronization state between memories, much less any type of signal indicating that memories are at a common synchronization state. Therefore, Huang fails to teach or suggest "asserting a synchronization signal indicating that the group of memories are at a common synchronization state," as recited in independent claim 19. Therefore, Huang cannot cure the deficiencies of the FIG. 1 Art. Accordingly, Applicants respectfully request that the 35 U.S.C. § 103(a) rejection based upon the FIG. 1 Art and Huang be withdrawn from independent claim 19.

Because each of the cited references, individually and in combination, fails to teach or suggest "asserting a synchronization signal indicating that the group of memories are at a common synchronization state," as recited in independent claim 19, the 35 U.S.C. § 103(a) rejections should be withdrawn.

Dependent claims 20-29 depend from independent claim 19 and are allowable for at least the reasons recited above in support of their parent claim 19. They are also independently patentable. Accordingly, the 35 U.S.C. § 103(a) rejections of claims 20-29 should be withdrawn.

d. Claims 30, 32 (first claim 32), and 37

Independent claim 30 as amended is directed to a method of testing memories, and requires: "coupling a resume input on the integrated circuit to the first and second BIST controllers."

The FIG. 1 Art fails to teach or suggest a method of testing memories requiring coupling a resume input on the integrated circuit to the first and second BIST controllers, such as recited in independent claim 30. The FIG. 1 Art describes FIG. 1 as showing that "each BIST controller is coupled to a separate "hold" pin, such as hold pins 30, 32, on the IC 14" (see page 3, lines 17-

18), but it explicitly lacks any type of resume pin for any of the N BIST controllers, much less a resume pin coupled to multiple BIST controllers. Therefore, the FIG. 1 Art fails to teach or suggest "coupling a resume input on the integrated circuit to the first and second BIST controllers," as recited in independent claim 30.

Phan does not cure the deficiencies of the FIG. 1 Art. Phan also fails to teach or suggest a method of testing memories requiring coupling a resume input on the integrated circuit to the first and second BIST controllers, such as recited in independent claim 30. Phan does disclose a BIST controller 102 (see FIG. 1) having multiple inputs but is understood to disclose nothing relating to any type of resume input to the BIST controller, much less any type of resume input coupled to multiple BIST controllers. For example, Phan states: "the BIST state machine/controller 102 receives standard memory address bus signals MEMORY ADDRESS, data bus signals MEMORY DATA_IN and control signals MEMORY CONTROL provided by other components or input pins of the integrated circuit IC" and "[a] system clock signal SYSTEM_CLOCK is also provided" (Phan at col. 6, lines 30-34 and 57-60, respectively). None of these inputs represents a resume input because they represent other types of inputs (e.g., address). Therefore, Phan fails to teach or suggest "coupling a resume input on the integrated circuit to the first and second BIST controllers," as recited in independent claim 30. Therefore, Phan cannot cure the deficiencies of the FIG. 1 Art. Accordingly, Applicants respectfully request that the 35 U.S.C. § 103(a) rejection based upon the FIG. 1 Art and Phan be withdrawn from independent claim 30.

Huang also does not cure the deficiencies of the FIG. 1 Art. Huang also fails to teach or suggest a method of testing memories requiring coupling a resume input on the integrated circuit to the first and second BIST controllers, such as recited in independent claim 30. Huang does

disclose a BIST controller 22 (see FIG. 1) having multiple inputs but is understood to disclose nothing relating to any type of resume input to the BIST controller, much less any type of resume input coupled to multiple BIST controllers. For example, Huang states: "the state transitions are controlled by the BIST control section input BCS," "[a]n activation control signal BAC connected to the BIST controller 22 is at a logical zero when the DRAM is in normal operations and goes high to a logical one to activate the BIST logic to test the embedded DRAM 13," and "[t]he BRS input signal to the BIST controller 22 resets the BIST and implements a scan of all registers in the BIST controller 22 and the logic in the memory BIST 10 excluding the BIST controller 22" (Huang at col. 4, lines 39-40, 43-47, and 55-58, respectively). None of these inputs represents a resume input because they each represent other types of inputs (e.g., state transitions). Therefore, Huang fails to teach or suggest "coupling a resume input on the integrated circuit to the first and second BIST controllers," as recited in independent claim 30. Therefore, Huang cannot cure the deficiencies of the FIG. 1 Art. Accordingly, Applicants respectfully request that the 35 U.S.C. § 103(a) rejection based upon the FIG. 1 Art and Huang be withdrawn from independent claim 30.

Because each of the cited references, individually and in combination, fails to teach or suggest "coupling a resume input on the integrated circuit to the first and second BIST controllers," as recited in independent claim 30, the 35 U.S.C. § 103(a) rejections should be withdrawn.

Dependent claims 32 and 37 (formerly the second claim 32) depend from independent claim 30 and are allowable for at least the reasons recited above in support of their parent claim 30. They are also independently patentable. Accordingly, the 35 U.S.C. § 103(a) rejections of claims 32 and 37 should be withdrawn.

Claims 31 and 33 and the second claim 32 have been canceled, thereby rendering the rejections of claims 31 and 33 and the second claim 32 moot.

e. Claims 34-36

Independent claim 34 is directed to a computer readable medium on which is stored a software tool that inserts BIST controllers into circuits that test memory elements, and requires: "reading a description of a user-defined test algorithm for a BIST controller, wherein the algorithm includes having the BIST controller enter into one or more synchronization states in which the controller enters an idle state" (emphasis added).

The FIG. 1 Art of the present application fails to teach or suggest a software tool stored on a computer readable medium that requires reading a description of a user-defined test algorithm for a BIST controller, wherein the algorithm includes having the BIST controller enter into one or more synchronization states in which the controller enters an idle state, such as recited in independent claim 34. For example, the FIG. 1 Art does not show or suggest anything related to synchronization states, much less synchronization states of BIST controllers. Therefore, the FIG. 1 Art fails to teach or suggest "reading a description of a user-defined test algorithm for a BIST controller, wherein the algorithm includes having the BIST controller enter into one or more synchronization states in which the controller enters an idle state," as recited in independent claim 34.

Phan does not cure the deficiencies of the FIG. 1 Art. Phan also fails to teach or suggest a software tool stored on a computer readable medium that requires reading a description of a user-defined test algorithm for a BIST controller, wherein the algorithm includes having the BIST controller enter into one or more synchronization states in which the controller enters an

idle state, such as recited in independent claim 34. The only reference understood to be present in Phan to anything related to synchronization is as follows: "A **system clock signal** SYSTEM_CLOCK is also provided to both the BIST state machine controller 102 and the BISR circuitry 110 for logic clocking and synchronization" (Phan at col. 6, lines 57-60, emphasis added). Thus, Phan describes a system clock signal that is input to a BIST but is understood to disclose nothing related to synchronization states, much less synchronization states of BIST controllers. Therefore, Phan fails to teach or suggest "reading a description of a user-defined test algorithm for a BIST controller, wherein the algorithm includes having the BIST controller enter into one or more synchronization states in which the controller enters an idle state," as recited in independent claim 34. Therefore, Phan cannot cure the deficiencies of the FIG. 1 Art. Accordingly, Applicants respectfully request that the 35 U.S.C. § 103(a) rejection based upon the FIG. 1 Art and Phan be withdrawn from independent claim 34.

Huang also does not cure the deficiencies of FIG. 1. Huang also fails to teach or suggest a method of testing a group of memories requiring asserting a synchronization signal indicating that the group of memories are at a common synchronization state, such as recited in independent claim 34. The only reference understood to be present in Huang to anything related to synchronization is as follows: "All signals are synchronized **with the BIST clock**, BCK" (Huang at col. 5, line 65, emphasis added). Thus, Huang describes a clock signal that is input to a BIST but is understood to disclose nothing related to synchronization states, much less synchronization states of BIST controllers. Therefore, Huang fails to teach or suggest "reading a description of a user-defined test algorithm for a BIST controller, wherein the algorithm includes having the BIST controller enter into one or more synchronization states in which the controller enters an idle state," as recited in independent claim 34. Therefore, Huang cannot cure the deficiencies of

the FIG. 1 Art. Accordingly, Applicants respectfully request that the 35 U.S.C. § 103(a) rejection based upon the FIG. 1 Art and Huang be withdrawn from independent claim 34.

Because each of the cited references, individually and in combination, fails to teach or suggest "reading a description of a user-defined test algorithm for a BIST controller, wherein the algorithm includes having the BIST controller enter into one or more synchronization states in which the controller enters an idle state," as recited in independent claim 34, the 35 U.S.C. § 103(a) rejections should be withdrawn.

Dependent claims 35 and 36 depend from independent claim 34 and are allowable for at least the reasons recited above in support of their parent claim 34. They are also independently patentable. Accordingly, the 35 U.S.C. § 103(a) rejections of claims 35 and 36 should be withdrawn.

III. Claim Objections

The Office Action objected to claim 4, stating that line 2 should be amended to read "and further" rather than "and the further." Such amendment has been made. Thus, Applicants respectfully request that the objection be removed.

The Office Action also objected to claims 35 and 36, stating that they should be amended to properly depend from claim 34 instead of claim 26. Such amendments have been made. Thus, Applicants respectfully request that the objections be removed.

IV. Request for Examiner Interview

If any issues remain, the Examiner is formally requested to contact the undersigned prior to issuance of the next Office Action in order to arrange for a telephonic interview. It is believed

that a brief discussion of the merits of the present application may expedite prosecution. This request is being submitted under MPEP § 713.01, which indicates that an interview may be arranged in advance by a written request.

V. Conclusion

The present application is now in condition for allowance and such action is respectfully requested.

Respectfully submitted,

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